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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/657,139	09/09/2003	Shinji Ohuchi	KKH.039D2	1910

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EXAMINER	
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ART UNIT	PAPER NUMBER
2893	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/657,139	OHUCHI ET AL.	
	Examiner	Art Unit	
	DILINH P. NGUYEN	2893	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 October 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *34-37,46 and 53-61* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *34-37,46 and 53-61* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 09/757,663.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *1/12/09*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 34, 37, 46, 53 and 57-61 are rejected under 35 U.S.C. 103(a) as being unpatentable over Egawa (U.S. Pat. 6229215) in view of Buckley, III et al. (U.S. Pat. 5477082).

Regarding claim 34, Egawa et al. disclose a semiconductor device (figs. 2 and 4) comprising:

a BGA (ball grid array) type semiconductor device including a base plate 10 (fig. 2) or a base plate 30 (fig. 4), a first resin 22 (fig. 2) that seals a frontside surface of the base plate, and a plurality of bumps 15 formed on a backside surface of the base plate that is opposite the frontside surface (figs. 2 or 4); and

a CSP (chip size packaged) type semiconductor device mounted on an area of the backside surface of the base plate of the BGA type semiconductor device which does not have the plurality of bumps formed thereon (fig. 4),

the CSP type semiconductor device having a semiconductor element 17 which has main and back surface, and side surfaces between the main and back surfaces, and a plurality of terminals 18 which are formed on the main surface (fig. 4),

wherein the back surface and the entirety of the side surfaces of the semiconductor element 17 are exposed (fig. 4),

the CSP type semiconductor device as mounted on the backside surface of the base plate 30 has a thickness less than a thickness of plurality of bumps 15 (fig. 4), and

wherein the CSP type semiconductor device has a second resin that covers the main surface of the semiconductor element 17 and side surfaces of the terminals 18, the first and second resins are separate from each other (fig. 2);

Egawa et al. do not disclose a printed circuit board via the plurality of bumps.

However, Buckley, III et al. disclose a semiconductor device (cover fig.) comprising: a base plate 60 and a plurality of bumps 54 formed on the base plate 60, wherein the backside surface of the base plate 60 is mounted to a printed circuit board 52 (column 3, line 33) via the plurality of bumps 54 (cover fig.).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to form a printed circuit board is mounted to the backside surface of the base plate via the plurality of bumps as taught by Buckley, III et al. into the device of Egawa et al. in order to provide a electrical connection for the plurality of bumps and different application for the semiconductor package (cover fig.).

Regarding claim 37, Egawa discloses that the CSP type semiconductor device is mounted on the BGA type semiconductor device so that a front surface of the CSP type semiconductor device faces the backside surface of the base plate 30 (fig. 4).

Regarding claim 46, Egawa et al. disclose that wherein the main surface of the semiconductor element 17 faces the backside surface of the base plate 30 (fig. 4).

Regarding claim 53, Egawa et al. disclose a semiconductor device (figs. 2 and 4) comprising:

a BGA (ball grid array) type semiconductor device including a base plate 10 (fig. 2) or a base plate 30 (fig. 4), a first resin 22 (fig. 2) that seals a frontside surface of the base plate, and a plurality of bumps 15 formed on a backside surface of the base plate that is opposite the frontside surface (figs. 2 or 4); and

a CSP (chip size packaged) type semiconductor device mounted on an area of the backside surface of the base plate of the BGA type semiconductor device which does not have the plurality of bumps formed thereon (fig. 4),

the CSP type semiconductor device having a semiconductor element 17 which has main and back surface, and side surfaces between the main and back surfaces, and a plurality of terminals 18 which are formed on the main surface (fig. 4),

wherein the back surface and the entirety of the side surfaces of the semiconductor element 17 are exposed (fig. 4),

wherein the main surface of the semiconductor element 17 is sealed with a second resin, and portions of each of the plurality of terminals 18 are exposed from the second resin (a surfaces are connecting with the plate 10 that are exposed form the

second resin), the first resin 22 and the second resin are separate from each other (fig. 2) and

the CSP type semiconductor device as mounted on the backside surface of the base plate has a thickness less than a thickness of plurality of bumps 15 (fig. 2).

Egawa et al. do not disclose a printed circuit board via the plurality of bumps.

However, Buckley, III et al. disclose a semiconductor device (cover fig.) comprising: a base plate 60 and a plurality of bumps 54 formed on the base plate 60, wherein the backside surface of the base plate 60 is mounted to a printed circuit board 52 (column 3, line 33) via the plurality of bumps 54 (cover fig.).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to form a printed circuit board is mounted to the backside surface of the base plate via the plurality of bumps as taught by Buckley, III et al. into the device of Egawa et al. in order to provide a electrical connection for the plurality of bumps and different application for the semiconductor package (cover fig.).

Regarding claims 57 and 60, Egawa discloses that the BGA type semiconductor device has a semiconductor element 11 sealed within the first resin 22 (fig. 2) and it would have been obvious to one having ordinary skill in the art to have a size of the semiconductor element of the BGA type semiconductor device is smaller than a size of the semiconductor element of the CSP type semiconductor device. Note *Inaba et al. (fig. 9)* is cited to support for the well known position.

Regarding claim 58, Egawa et al. disclose that wherein the BGA type semiconductor device and the CSP type semiconductor deice are individually manufactured.

Regarding claims 59 and 61, Egawa et al. disclose that wherein the BGA type semiconductor device has a semiconductor element 11 sealed within the first resin 22 which has a thickness greater than a thickness of the semiconductor element 17 of the CSP type semiconductor device (fig. 2).

3. Claims 35-36 and 54-56 are rejected under 35 U.S.C. 103(a) as being unpatentable over Egawa (U.S. Pat. 6229215) in view of Buckley, III et al. (U.S. Pat. 5477082) as applied to claims 34 and 53 above, and further in view of Lin et al. (U.S. 5239198).

Regarding claims 35 and 54, as discussed in details above, Egawa and Buckley, III et al. substantially disclose all the limitations as claimed above except for a plurality of conductive portions on the backside surface of the base plate, the semiconductor device further comprising a plurality of conductive members, each of which is located between a corresponding one of the plurality of conductive portions and the portion of a corresponding one of the plurality of terminals.

However, Lin et al. disclose a semiconductor device comprising: a plurality of conductive portions 42 (fig. 5, column 6, lines 33-34) on the backside surface of the base plate 12, the semiconductor device further comprising a plurality of conductive members 16, each of which is located between a corresponding one of the plurality of

conductive portions and the portion of a corresponding one of the plurality of terminals 51 (fig. 6).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the device of Egawa and Buckley, III et al. by having a plurality of conductive portions on the backside surface of the base plate, the semiconductor device further comprising a plurality of conductive members, each of which is located between a corresponding one of the plurality of conductive portions and the portion of a corresponding one of the plurality of terminals as taught by Lin et al., such a plurality of conductive portions and conductive members would provide external electrical connections to the device (fig. 6).

Regarding claim 36, Egawa et al. disclose that wherein the plurality of terminals 18 of the CSP type semiconductor device 17 are coupled to the wiring patterns via solder joints (fig. 4, column 5, lines 35-41).

Regarding claim 55, Lin et al. disclose that the conductive members 16 are not sealed with the first and second resin (fig. 6).

Regarding claim 56, Line et al. disclose that the conductive portions 42 are solder (column 6, lines 33-34).

Response to Arguments

The applicant amended claims 34, 53, 55, 57 and 61. Please see the rejection regarding the currently amended claims 34 and 53 above.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to DILINH P. NGUYEN whose telephone number is (571) 272-1712. The examiner can normally be reached on 9:00 AM - 6:30 PM (Monday-Thursday).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Davienne Monbleau can be reached on (571) 272-1945. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

DLN

1/21/09

/A. Sefer/
Primary Examiner
Art Unit 2893